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10/674,886	09/30/2003	Hyunjun Kim	P16828	9223

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED

1 2 2006

GROUP 2800

Application Number: 10/674,886
Filing Date: September 30, 2003
Appellant(s): KIM ET AL.

Patrick J. Buckley (40,928)
For Appellant

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SEP 1 1 2006

GROUP 2800

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12 June 2006 appealing from the Office action mailed 11 January 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct. Although Applicant has added extra information for the sake of clarity, Applicant does state each of the limitations of the sole independent claim, claim 1. Specifically, regarding claim 1, Applicant states an apparatus comprising: a first voltage plane having a first conducting portion to be at a first voltage (pg. 2 of the Brief, final paragraph, lines 1-4) a signal layer on one side of the first voltage plane (pg. 2 of the Brief, final paragraph, lines 4-5); a second voltage plane on the other side of the first voltage plane

and having a second conducting portion to be at a second voltage (pg. 2 of the Brief, final paragraph, line 5 – pg 3, same paragraph, line 7); and a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is, (i) electrically connected to the second conducting portion at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end (pg. 3 of the Brief, same paragraph, lines 7-11). No dependent claim is argued separately.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5, 7-16, and 18-21 are rejected under 35 USC 103 as being unpatentable over US 6,172,305 B1 (Tanahashi).

(10) Response to Argument

Firstly, Applicant alleges, referring to page 3 of Applicant's Brief, "neither P2 nor layer 12 is a voltage plane". Although Applicant admits that layer 12 does contain a conductive portion set to a specific voltage (i.e. P2), Applicants seem to allege that the presence of additional conductive portion G2 on layer 12, would prevent the ordinarily skilled artisan from recognizing layer 12 as a "first voltage plane". However, the Examiner asserts that Applicant has provided no specific special definition to the term "first voltage plane" and further that in determining the broadest reasonable interpretation of the term "first voltage plane" consistent with the specification, the ordinarily skilled artisan would define "first voltage plane" as simply a first plane, which provides a voltage. Indeed, it is clear that the layer 12, as disclosed in figures 3A – 3C of Tanahashi is, in fact a planar object, which provides a voltage via the conductive portion P2 (see also col. 14, lines 40-50). Thus, it is the Examiner's position that the instantly claimed "first voltage plane" is indeed taught by Tanahashi. The presence of other types of wiring (e.g. ground wiring G2) does not prevent the layer 12 from performing as a first voltage plane.

Secondly, and similarly, Applicant alleges, referring to page 3 of Applicant's Brief, "layer 11 is not a voltage plane". Although Applicant admits that layer 11 does contain a conductive portion set to a specific voltage (i.e. G1), Applicants seem to allege that the presence of additional conductive portions P1 and S1 on layer 11, would prevent the ordinarily skilled artisan from recognizing layer 11 as a "second voltage plane". However, the Examiner asserts that Applicant has provided no specific special definition to the term "second voltage plane" and further that in determining the broadest

reasonable interpretation of the term "second voltage plane" consistent with the specification, the ordinarily skilled artisan would define "second voltage plane" as simply a second plane, which provides a voltage. Indeed, it is clear that the layer 11, as disclosed in figures 3A – 3C of Tanahashi is, in fact a planar object, which provides a voltage via the conductive portion G1 (see also col. 14, lines 40-50). Thus, it is the Examiner's position that the instantly claimed "second voltage plane" is indeed taught by Tanahashi. The presence of other types of wiring (e.g. power wiring P1 and signal wiring S1) does not prevent the layer 11 from performing as a second voltage plane.

Thirdly, Applicant alleges that Tanahashi does not teach the limitation "a 'plurality' of floating microstrip line traces on the signal layer". Applicant asserts that the passage from col. 16, lines 55-60 which states:

> Further, a plurality of wiring conductors may be placed for each kind, and various multilayer circuit boards configured by the first to four insulating layers I1 to I4 may be combined and overlaid on the multiplayer circuit board configured by the first to fourth insulating layers I1 to I3.

"refers to additionally layers being added to the circuit board and does not disclose or suggest that a plurality of floating microstrip lines may be provided on the signal layer as recited in the claims" (emphasis Applicant's). The Examiner agrees that the "various multilayer circuit boards configured by the first to four insulating layers I1 to I4 may be combined and overlaid on the multiplayer circuit board configured by the first to fourth insulating layers I1 to I3" portion does indeed teach additional circuit layers. However, the portion that reads, "a plurality of wiring conductors may be placed for each kind", teaches that for each kind of wiring conductor disclosed in the invention a plurality of

such conductors may be provided. Thus, this passage would suggest to the ordinarily skilled artisan that though only one of any such wiring is expressly depicted in the figures, multiple such wiring is contemplated. As the Examiner has stated in the Final Rejection, Tanahashi does indeed expressly show one such floating microstrip line trace (G4) on the signal layer. And though not shown in the figures, as stated in the above quoted passage from col. 16, lines 55-60, a plurality of such floating microstrip line traces is contemplated.

Thus, having addressed each of Applicant's arguments, the Examiner asserts that the traversal of the Final Rejection on these grounds is unsuccessful and respectfully submits that the Final Rejection should be affirmed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jeremy C. Norris

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